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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/718,563 | 11/24/2003 | Takashi Kobayashi | XA-9997 | 1857 |

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| EXAMINER | |
|---|---|
| DICKEY, THOMAS L | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2826 | |

DATE MAILED: 12/09/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/718,563 | KOBAYASHI ET AL. | |
| | Examiner | Art Unit | |
| | Thomas L Dickey | 2826 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *05 October 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4-7 and 10* is/are rejected.

7)☒ Claim(s) *2,3,8,9 and 11* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 November 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/24/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

**1.** The preliminary amendment filed on 11/24/2003 has been entered.

### *Election/Restriction*

**2.** On 9/16/04 Applicant was subjected to a restriction requirement between the invention of claims 1-11 and the invention of claims 12-16. Applicant correctly points out that claims 12-16 were cancelled by preliminary amendment. This having been done, there is no basis for the restriction requirement of 9/16/04. Action on the merits is forthcoming.

### *Oath/Declaration*

**3.** The oath/declaration filed on 03/17/2004 is acceptable.

### *Drawings*

**4.** The drawings are objected to as follows:

**A.** Figure 15 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). This objection to the drawings will not be held in abeyance.

**B.** The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description: 127. This objection to the drawings will not be held in abeyance.

**C.** The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the "split channel formed within said semiconductor substrate," (claim 4), "split channel" (claim 5), and "contact hole made through a third dielectric film formed on said third gate," said contact hole being provided on "a member having the same material and film thickness as a film that forms said second gate" (claim 8 – note that figure 2 shows a contact hole 128 but there is no drawing showing it being made through "a third dielectric film formed on said third gate," nor is there a drawing showing it being provided on "a member having the same material and film thickness as a film that forms said second gate") must be shown or the feature(s) canceled from the claim(s). No new matter should be entered. This objection to the drawings will not be held in abeyance.

**D.** With regard to the objections enumerated above corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary,

the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the examiner does not accept the changes, the applicant will be notified and informed of any required corrective action in the next Office action. The objections to the drawings will not be held in abeyance.

***Priority***

**5.** Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

***Information Disclosure Statement***

**6.** The Information Disclosure Statement filed on 11/24/2003 has been considered.

***Specification***

**7.** The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of

the following is required: The specification must provide proper antecedent basis for the "split channel formed within said semiconductor substrate," (claim 4), "split channel" (claim 5) and the "contact hole made through a third dielectric film formed on said third gate," said contact hole being provided on "a member having the same material and film thickness as a film that forms said second gate" (claim 8). Until applicant provides a different explanation, it will be assumed that the claim 4 language "wherein said second gate controls a split channel formed within said semiconductor channel," and the claim 5 language "split channel," simply means that the first and second gates "split" close adjacency (via first and second gate dielectrics) to the channel, so that both gates must be "on" to create a channel that extends all the way from the source to the drain so as to allow source/drain conductance. This is a well-known concept amongst those familiar with the art, typically called a "split gate." Note prior art figure 3 of Eitan et al. 4,998,220, showing a first gate 64 overlying a first portion 53 of a channel, and second gate 58 overlying a second portion 57 of the channel.

***Claim Objections***

**8.** Claims 1,8, and 10-11 are objected to because of the following informalities:

**A.** The claim language "a channel region," is used three times (on lines 6,8, and 11 of claim 1 and lines 8,10, and 13 of each of claims 8 and 10) in each of claims 1,8, and 10. It appears to have been applicants' intention to claim but a single channel region in each claim. These claims will be examined under the assumption that this was

applicants' intent. To clearly express this intent applicants must amend the second and third references to the channel region to read "the channel region," or "said channel region," instead of "a channel region," in each independent claim 1,8, and 10. If applicants intend to claim three channel regions in each claim applicants must use three distinct names for them.

**B.** In claim 8, the claim language "a third dielectric film," is used twice, first on lines 17-18 and again on lines 21-22. It appears from context that the "third dielectric film" of lines 17-18 is a distinct element from the "third dielectric film" of lines 21-22. Applicant is required to use claim language that clearly distinguishes these elements, for example, "a third dielectric film," and "a fourth dielectric film."

**C.** In claim 10 line 10, applicants recite "first gate that is provided in a channel region." In line 13, applicants recite "second gate that is provided in a channel region." In this case it appears that applicants intended to recite "above" instead of "in," as they do in claims 1 and 8. If applicants insist on claim language requiring gates to be in a channel applicants will be required, under 35 USC 112, to supply a teaching that shows one of ordinary skill in the art how to make such gates functional.

**D.** In claim 11 line 2, it appears that applicants introduce "an impurity diffusion layer." Applicants already introduced "an impurity diffusion layer" in claim 10, from which claim 11 depends. Applicants must re-name the "impurity diffusion layer" of claim 11 in order to distinguish it from the "impurity diffusion layer" that is already in this claim by way of incorporating claim 10 by reference.

Appropriate correction is required.

***Claim Rejections - 35 USC § 102***

**9.** The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1,4, and 5 rejected under 35 U.S.C. 102(b) as being anticipated by SHIN (6,476,440).

Shin discloses a nonvolatile semiconductor memory device with a source region 41a and a drain region 41b that are positioned at a specified distance from each other; a main surface of a semiconductor substrate 31; a channel region that is formed between said source region 41a and said drain region 41b; a first gate 39 that is provided above said channel region on a side toward said drain region 41b and via a first gate dielectric film 38a; a second gate 33a-35a that is provided above said channel region on a side toward said source via a second gate dielectric film 32, wherein a lateral surface of said second gate 33a-35a is covered with a first dielectric film 36a and an upper surface of said second gate 33a-35a is provided with a second dielectric film 37; wherein: the source region 41a and the drain region 41b are mounted on the main surface of the semiconductor substrate 31; said first gate 39 is formed so as to cover said first gate dielectric film 38a, the lateral surface of said first dielectric film 36a, and the lateral

surface of said second dielectric film 37; one end of said first gate 39 is positioned on an upper end face of said second dielectric film 37; wherein said channel region is "split" into two regions, one of which is controlled by said second gate 33a-35a via said second gate dielectric film 32.and said second gate 33a-35a has a gate function for controlling both an erase gate 35a and as the floating gate 33a half of a split gate (split channel, in applicants unique terminology). Note figure 4e and column 5 lines 3-57 of Shin.

***Claim Rejections - 35 USC § 103***

**10.** The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 6 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over SHIN (6,476,440) in view of KOBAYASHI (2001/0045590).

Shin discloses a nonvolatile semiconductor memory device with all the limitations of claims 6 and 7 except that said second gate dielectric film is the same as a gate dielectric film for a MOS transistor that composes a low-voltage section of a peripheral circuit formed on said semiconductor substrate (claim 6) and that the material and film thickness of said second gate are the same as those of a gate for a MOS transistor that

composes said peripheral circuit formed on said semiconductor substrate. Note figure 4e and column 5 lines 3-57 of Shin.

However, Kobayashi discloses a nonvolatile semiconductor memory device with a second gate dielectric film 109 that is the same as a gate dielectric film 109 for a MOS transistor that composes a low-voltage section of a peripheral circuit formed on a semiconductor substrate (claim 6) and that the material and film thickness of a second non-volatile memory transistor gate 110a are the same as those of a gate 110b for a MOS transistor that composes the peripheral circuit formed on the semiconductor substrate. Note figures 2A-2D and paragraphs 150-152 of Kobayashi. Therefore, it would have been obvious to a person having skill in the art to replace the second gate dielectric film and second gate of Shin's nonvolatile semiconductor memory device with the with the second gate dielectric film that is the same as a gate dielectric film for a MOS transistor that composes a low-voltage section of a peripheral circuit formed on said semiconductor substrate (claim 6) and the second gate having material and film thickness that are the same as those of a gate for a MOS transistor that composes said peripheral circuit formed on said semiconductor substrate, such as taught by Kobayashi in order to allow the nonvolatile semiconductor memory device to be assembled at the same time as the MOS transistors that compose the peripheral circuit to thus provide a more efficient method of manufacturing a device including memory and peripheral circuits for accessing the memory.

**A.** Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over SHIN (6,476,440) in view of HARARI ET AL. (6,103,573).

Shin discloses a nonvolatile semiconductor memory device with a source region 41a and a drain region 41b that are positioned at a specified distance from each other; a main surface of a semiconductor substrate 31; a channel region that is formed between said source region 41a and said drain region 41b; a first gate 39 that is provided above said channel region on a side toward said drain region 41b and via a first gate dielectric film 38a; a second gate 33a-35a that is provided above said channel region on a side toward said source via a second gate dielectric film 32, wherein a lateral surface of said second gate 33a-35a is covered with a first dielectric film 36a and an upper surface of said second gate 33a-35a is provided with a second dielectric film 37; wherein a third gate 42 is provided via a third dielectric film 40 formed on said first gate 39; and a bind region (see alternate cross-section 4b – the bind region is the region that lines 33 and 35 and insulators 32 and 34 pass through, at right angles to gate/wordlines 42) for binding a plurality of said second gates 33a-35a is provided on a region (said region being the top surface region) of said semiconductor substrate 31 where an impurity diffusion layer 33 including a second conductivity type (n-type) is selectively formed. Note figures 4b, 4e and column 5 lines 3-57 of Shin. Shin does not disclose that the source region and the drain region are formed in a first conductive well.

However, Harari et al. discloses a nonvolatile semiconductor memory device with source and drain regions formed in a first conductive well. Note column 9 lines 59-64 of

Harari et al. Therefore, it would have been obvious to a person having skill in the art to augment Shin's nonvolatile semiconductor memory device with the source and drain regions formed in a first conductive well such as taught by Harari et al. in order to use said well to isolate the source and drain pairs from other memory blocks formed on the chip to thus allow one block of memory to be erased independently of others.

***Allowable Subject Matter***

**11.** Claims 8 and 9 are objected to for the reasons set forth in Section 8 above. Should Applicants amend claim 8 to clearly express their intended meaning (as that meaning is currently understood) claims 8 and 9 appear allowable.

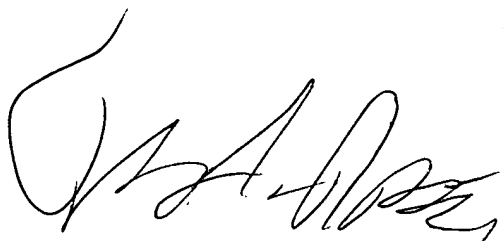
**12.** Claims 2,3, and 11 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Applicants should take note that the base claims, claims 1 and 10, contains language objected to in Section 8, above. Applicants must amend claims 1 and 10 to clearly express their intended meaning before copying the language of claims 1 and 10 to re-write claims 2,3, and 11 in independent form.

***Conclusion***

**13.** Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas L Dickey whose telephone number is 571-272-1913. The examiner can normally be reached on Monday-Thursday 8-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



**Thomas L. Dickey**
**Patent Examiner**
**Art Unit 2826**
**12/04**